REMARKS/ARGUMENTS

Claims 1-20 are pending in the present application. Reconsideration of the claims is respectfully requested.

I. 35 U.S.C. § 102, Anticipation

The examiner has rejected claims 1-3, 8-13, and 17-20 under 35 U.S.C. § 102 as being anticipated by U.S. Patent Application Publication 2004/0187049 published by *West*. This rejection is respectfully traversed.

Applicant's independent claims describe generating logical ones using pulses that are a first length and generating logical zero pulses that are a second length.

The Examiner states that *West* describes these features on pages 3-4 in paragraph 0045 and in Figure 3b. Applicant disagrees.

Paragraph 0045 teaches comparing two voltage levels to determine whether a logic state of zero or a logic state of one will be output. Figure 3b teaches particular voltage levels and the resulting outputs for those voltage levels. Neither paragraph 0045 nor Figure 3b, however, teaches the length of pulses. Neither Figure 3b or paragraph 0045 teaches logical ones that are a first length and logical zeros that are a second length.

More particularly, paragraph 0045 teaches that output ra has a logic state of one if Vra is greater than Vofa and a logic state of zero if Vra is not greater than Vofa. The output rb has a logic state of one if Vrb is greater than Vofb and a logic state of zero if Vrb is not greater than Vofb. Figure 3b provides example values for Vra, Vrb, Vofa, and Vofb and the resulting ra and rb outputs.

Applicant teaches logical one pulses that are a first length and logical zero pulses that are a second length. *West* does not provide any teaching at all as to pulse length. *West* teaches using voltage levels to determine whether a logical one or logical zero will be output. *West*, however, does not teach what the logical one and logical zero pulses will look like. *West* provides no teaching regarding the parameters of logical one and logical zero pulses.

Applicant claims pulses that have particular parameters. As Applicant's claims describe, the logical ones are pulses that are a first length and logical zero pulses are a second length. Nothing in *West* teaches logical ones that are pulses that are a first length and logical zero pulses that are a second length.

Because *West* does not teach logical one pulses that are a first length and logical zeros that are a second length, *West* does not anticipate Applicant's claims.

Since the remaining claims depend from the independent claims discussed above, the remaining claims are patentable for the reasons given above.

II. **Objection to Claims**

The examiner has stated that claims 4-7 and 14-16 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The Examiner stated that the prior art failed to disclose the combination of the base claim, the features of claim 3; and the features of: connecting a first node of a second resistor included within said external device to a power source; connecting a second node of said second resistor to a first node of an LED; connecting a second node of said LED to a first communication pin of said external device; connecting said second node of said LED to a first node of a switch; and connecting a second node of said switch to ground.

Claim 13 describes the combination of the base claim, features of claim 12 which are similar to claim 3, and a first node of a second resistor included within said external device connected to a power source; a second node of said second resistor connected to a first node of an LED; a second node of said LED connected to a first communication pin of said external device; said second node of said LED connected to a first node of a switch; and a second node of said switch connected to ground. Claim 13 includes features that are similar to claim 4. The examiner stated that claim 4 was merely objected to and not anticipated by *West*. Because claim 13 includes features that are similar to claim 4 , Applicant believes that claim 13 is not anticipated by *West*.

Further, although claim 13 is indicated as being anticipated by *West*, the Examiner provides no explanation as to why *West* anticipates claim 13.

Therefore, Applicant believes claim 13 is not anticipated by *West*.

III. Conclusion

It is respectfully urged that the subject application is patentable over *West* because *West* does not teach generating logical ones using pulses that are a first length and generating logical zeros pulses that are a second length.

The examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: March 15, 2006

Respectfully submitted,

Lisa L. B. Yociss
Reg. No. 36,975
Yee & Associates, P.C.
P.O. Box 802333
Dallas, TX 75380
(972) 385-8777
Attorney for Applicant